

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT**

Title:

TOTAL INTERNAL REFLECTION (TIR) CMOS IMAGER

Inventor:

Tongbi Jiang, Mike Connell, and Jin Li

**Thomas J. D'Amico
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232**

TOTAL INTERNAL REFLECTION (TIR) CMOS IMAGER

FIELD OF THE INVENTION

[0001] The present invention relates to use of glass conductors as conductors of light to photo diodes in a CMOS chip, wherein said glass conductors are separated by at least one low refractive index material.

BACKGROUND OF THE INVENTION

[0002] There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photo diode arrays, charge injection devices and hybrid focal plane arrays. CCDs are often employed for image acquisition for small size imaging applications. CCDs are also capable of large formats with small pixel size and they employ low noise charge domain processing techniques. However, CCD imagers have a number of disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read out over time, they require good light shielding to avoid image smear and they have a high power dissipation for large arrays.

[0003] Because of the inherent limitations in CCD technology, there is an interest in complementary metal oxide semiconductor (CMOS) imagers for possible use as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications such as, for example, in cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems, star

trackers, motion detection systems, image stabilization systems and data compression systems for high-definition television.

[0004] A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photo diode, a photogate or a photoconductor overlying a doped region of a substrate for accumulating photo-generated charge in the underlying portion of the substrate.

[0005] In a conventional CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to a floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photo diode or a field induced depletion region beneath a photogate. For photo diodes, image lag can be eliminated by completely depleting the photo diode upon readout.

[0006] CMOS imagers have a number of advantages, including for example low voltage operation and low power consumption. CMOS imagers are also compatible with integrated on-chip electronics (control logic and timing, image processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data; and CMOS imagers have lower fabrication costs as compared with the conventional CCD since standard CMOS processing techniques can be used. Additionally, low power consumption is achieved for CMOS imagers because only one row of pixels at a time needs to be active during readout and there is no charge transfer (and associated switching) from

pixel to pixel during image acquisition. On-chip integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

[0007] With the need for enhanced resolution and a higher level of integration of an image array with associated processing circuit using CMOS imaging devices, there is a need for improving the characteristics of CMOS image arrays. As such, it would be beneficial to minimize if not eliminate the loss of light transmitted to pixel arrays during image acquisition. Enhanced light transmission upon pixel arrays is one means to enhance the image processing and imaging capabilities of CMOS chip devices. These enhancements in CMOS imagers have many applications, including use as imagers in color cameras.

[0008] Accordingly, there is needed an improved CMOS imaging device capable of receiving and propagating light to photo diodes with minimal loss of light transmission to the photo diodes. There is also needed an improved method for fabricating CMOS imaging devices, in which there is a high level of transmission of light to photo diodes and that reduces the drawbacks in CMOS imaging of the prior art. Methods of fabricating a pixel array exhibiting these improvements are also needed.

SUMMARY OF THE INVENTION

[0009] Embodiments of the present invention provide a CMOS imaging device, an image pixel array in a CMOS imaging device, and a CMOS imager system having improved characteristics for reception of light by photoconductors and transmission of this light to photo diodes. This enhanced reception of light by photoconductors is achieved by fabricating the photoconductors using one or more materials having a

refractive index greater than air. The photoconductors of the present invention are formed as individual units operable to transmit or propagate light directly to corresponding individual photo diodes. Also provided are methods for forming a CMOS imaging device, in accordance with embodiments of the present invention, comprising forming photoconductor arrays and at least one fluidic material in the intervening spaces between individual photoconductor units, wherein the fluidic material has a lower refractive index than the refractive index of the surrounding photoconductors.

[0010] In another embodiment of the invention, a method of fabricating a photoconductor array in a CMOS imaging device includes forming a plurality of photo diodes at or beneath the upper surface of a semiconductor substrate; exposing the upper surface of each of the photo diodes; forming a sacrificial layer over the photo diodes; removing at least a portion of said sacrificial layer to expose an opening over each of the photo diodes; forming a photoconductor over each photo diode; forming a color filter layer with an individual color filter over said each photo diode; forming a photoconductive layer over the color filter layer; and removing the sacrificial layer surrounding each photoconductor, where at least one fluidic material remains between each photoconductor, the fluidic material having a lower refractive index as compared to the refractive index of each photoconductor.

[0011] These and other features and advantages of the invention will be more apparent from the following detailed description that is provided in connection with the accompanying drawings and illustrated exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0012] Figure 1 depicts a schematic cross-sectional view of a portion of a CMOS chip device prior to the formation of a pixel array in accordance with one embodiment of the present invention.
- [0013] Figure 2 depicts a schematic cross-sectional view of the Figure 1 device at the beginning of the formation of a pixel array in accordance with the present invention and at an initial stage of processing.
- [0014] Figure 3 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 2.
- [0015] Figure 4 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 3.
- [0016] Figure 5 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 4.
- [0017] Figure 6 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 5.
- [0018] Figure 7 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 6.

[0019] Figure 8 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 7.

[0020] Figure 9 depicts a schematic cross-sectional view of the Figure 1 device formed at a stage of processing subsequent to that shown in Figure 8.

[0021] Figure 10 illustrates a schematic diagram of a computer processor system incorporating a CMOS imaging device fabricated according to the present invention, and wherein the CMOS imaging device contains one or more pixel arrays formed in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0022] In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural and logical changes may be made without departing from the spirit or scope of the present invention.

[0023] The terms “substrate” and “wafer” can be used interchangeably in the following description and may include any semiconductor-based structure. The structure should be understood to include silicon, silicon-on insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is

made to the substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0024] The term "metal" is intended to include not only elemental metal, but can include metal with other trace metals or in various alloyed combinations with other metals as known in the semiconductor art, as long as such alloy retains the physical and chemical properties of a metal. The term "metal" is also intended to include conductive oxides of such metals.

[0025] The term "pixel" refers to a discrete picture element unit cell containing a photoconductor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative photoconductor is illustrated in the figures and description herein. An array or combination of photoconductors together comprise a photoconductor array for use in a CMOS imager device. Typically, fabrication of all photoconductor arrays in an imager will proceed simultaneously in a similar fashion.

[0026] The term "sacrificial materials" refers to any material, for example, polynorbornene or polycarbonate based materials, that can readily decompose into volatile products when heated.

[0027] Now referring to the figures, where like reference numbers designate like elements, Figure 1 depicts a semiconductor substrate 110 in and on which a plurality of photo diodes 112 have been fabricated. The substrate 110 may comprise integrated circuits and other semiconductor components that may be incorporated in a CMOS chip device. Figure 1A depicts photo diodes 112 on the surface of the semiconductor substrate 110. In an alternate embodiment, Figure 1B

depicts photo diodes 112 beneath the surface of the substrate 110. Photo diodes 112 may be fabricated using conventional techniques and are shown to illustrate one environment of many in which the present invention may be employed.

[0028] The semiconductor photo diodes 112 of the present invention can mediate unidirectional current flow, as characteristic of diodes used in CMOS chip and imaging devices. For purposes of illustrating the invention, as depicted in Figures 1A-1B, photo diodes 112 are illustrated in a symmetric arrangement and orientation, with an intervening space separating each respective photo diode in substrate 110. It should be understood, however, that the invention is applicable to providing photo diodes in other arrangements and orientation, to be integrated with other components of a semiconductor device.

[0029] The process for making the structures illustrated in Figures 9A and 9B will now be described with reference to Figures 2-9. Figure 2A illustrates a substrate 110 along a cross-sectional view which is the same view as in Figure 1. For exemplary purposes, the substrate 110 may be a silicon substrate. However, as noted above, the invention has equal application to other semiconductor substrates.

[0030] In another embodiment of the invention, Figure 2B depicts in schematic manner openings which have been etched into substrate 110 and filled with photoconductive material 140. If the photo diodes 112 are beneath the surface of substrate 110, the first step in formation of a CMOS imaging device comprises etching away substrate 110 to form openings over each photo diodes 112, and to expose the upper surfaces of each photo diode 112 (not shown). This etching step may be formed by any conventional technique used for etching of semiconductor substrate materials. As illustrated in Figure 2B, this etching procedure, which

comprises removing a portion of the substrate 110, creates outer etched surfaces 126. These outer etched surfaces 126 mark the outer edges of the openings in which at least one sacrificial material 120 will be deposited within each opening over each respective photo diode 112.

[0031] In a preferred embodiment, the etched surfaces 126 are formed at an angle, to expose the upper surfaces of the photo diodes 112. Etching to form angled edges, as illustrated in Figure 2B, may be performed by angled-trench etching, for example.

[0032] The openings over each photo diode 112 are then filled with at least one sacrificial material 120. The application of sacrificial material 120 may be performed using conventional techniques, including for example surface micromachining processes. The sacrificial material may comprise any material that can readily decompose when heated, for example, polynorbornene or polycarbonate based materials. Other sacrificial materials, however, in addition to polynorbornene or polycarbonate based materials, can be used for the subject invention.

[0033] The sacrificial material 120 is then etched to remove at least a portion of the material 120 over the upper surfaces of the photo diodes 112, to form inner etched surfaces 132, as illustrated in Figure 2B.

[0034] As further depicted in Figure 2B, at least one photoconductive material 140 is then applied within the opening over each photo diode 112. The photoconductive material 140 may comprise any material that has a refractive index (n) greater than one ($n > 1$) and acts as a conductor of light or that can propagate or transmit light to an underlying photo diode 112. For example, the photoconductive material 140 may comprise nitride ($n=1.946$) or silicon dioxide (SiO_2) ($n=1.468$) at 550 nm wavelength.

[0035] In another embodiment, the photoconductors are broadly drawn to deposition of any type of "glass" conductive material (or glass conductor), and preferably to glass conductors with a refractive index greater than the refractive index of at least one fluidic material between each adjacent photoconductor. The combined fluidic materials have a refractive index lower than the refractive index of each of said photoconductors. The one or more fluidic materials between each adjacent photoconductor may comprise any gaseous or non-gaseous fluid.

[0036] Each photoconductor formed may receive and propagate light within an interior space of the photoconductor to at least one photo diode, wherein said interior space is defined by the outer surfaces of the photoconductor. The outer surfaces of each photoconductor may be of any configuration, including substantially straight, substantially diagonal, or curved. The image pixel array of the invention is preferably formed wherein there is minimal space between the upper portions of each adjacent photoconductor.

[0037] In one embodiment, the outer perimeter of an upper portion of each photoconductor may comprise at least three substantially straight edges. Alternatively, the outer perimeter of an upper portion of each photoconductor may be polygonal, substantially square, pentagonal, hexagonal, or octagonal. A nitride liner may also be provided around an outer perimeter of each photoconductor. In another embodiment, the diameter of an upper portion of each photoconductor may be greater than the diameter at the base of each respective photoconductor.

[0038] As illustrated in Figure 2A, at least one sacrificial material 124 is then applied over the upper surfaces of the photo diodes 112 and substrate 110. Alternatively, as illustrated in Figure 2B, the sacrificial material 124 can be applied over the upper surfaces of the etched sacrificial

material 120, the deposits of photoconductive material 140, and the upper surface of substrate 110.

[0039] As depicted in schematic form in Figure 3A, the step of etching and removing the sacrificial material 124 from over each of the plurality of photo diodes 112 comprises forming an etched opening 134 over each photo diode 112. In a preferred embodiment, there is minimal space along the length of an upper surface 136 of sacrificial material 124 that separates the upper portions of each adjacent opening 134.

[0040] Although Figure 3A depicts etched opening 134 as having substantially diagonal sidewall surfaces 138, it must be noted that the etched opening 134 is not limited in shape or dimensions to the depiction in the accompanying figures, but instead can be formed to any shape and dimensions desired. The etched opening 134 can, alternatively, have either concave or convex curved sidewall surfaces 138 that are substantially orthogonal to the generally horizontal planar surface of an upper surface 136 of sacrificial material 124.

[0041] Figure 3B illustrates an etched opening 134 formed over each deposit of photoconductive material 140, wherein each deposit of photoconductive material 140 has been deposited over each photo diode 112. As depicted in Figure 3B, it is desired to provide photo diodes 112 in an aligned manner to produce photoconductor arrays for maximal light absorption.

[0042] Figure 4A illustrates photoconductors 144 formed in accordance with one aspect of the present invention. After etched openings are formed, as depicted in Figures 3A and 3B, photoconductive

material is deposited or filled within each opening 134 to form photoconductors 144, with photoconductive layer 148. The photoconductors 144 may comprise any material that has a refractive index greater than one ($n > 1$) and acts as a conductor of light or that can propagate or transmit light to an underlying photo diode 112. For example, the photoconductors 144 may comprise either nitride ($n = 1.946$) or silicon dioxide (SiO_2) ($n = 1.468$) at 550 nm wavelength. Although in the preferred embodiment of the invention, nitride or silicon dioxide is used to form photoconductors 144, those skilled in the art will recognize that other compounds may be employed in place of nitride or silicon dioxide.

[0043] Nitride can act as a barrier in preventing contaminants from reaching the underlying photo diodes 112 or other integrated circuitry below the photo diodes, including circuitry integrated with the CMOS imaging device.

[0044] In one embodiment, as depicted in Figures 4A and 4B, the diameter of an upper portion of a photoconductor 144 is greater than the diameter of a base portion of the same photoconductor 144 formed over each photo diode 112. Although Figures 4A and 4B depict photoconductors 144 as having substantially diagonal sidewall surfaces, it must be noted that the photoconductors 144 are not limited in shape or dimensions to the depiction in the accompanying figures, but instead can be formed to any shape and dimensions desired. For example, photoconductors 144 can have either concave or convex curved sidewall surfaces that are substantially orthogonal to the generally horizontal planar surface of an upper surface 136 of sacrificial material 124.

[0045] At this stage, after forming photoconductors 144, chemical mechanical planarization (CMP) or other planarization may be used to planarize a photoconductive layer 148.

[0046] As illustrated in Figures 5A and 5B, a color resist layer 152, comprised of different color filters, is formed over photoconductive layer 148 and photoconductors 144. A single color filter is formed over each photoconductor 144. Since white light comprises red, green and blue light, it is preferred to form color resist layer 152 comprised of red, green and blue filters. In the case of a red filter placed over a photoconductor 144, for example, the red filter will absorb all colors of light except red, and thus only red light will pass through to the underlying photo diode 112. Any combination or array of color filters can be formed for color processing and imaging by a CMOS imaging device formed in accordance with the present invention.

[0047] In another embodiment (not shown), a color resist layer 152 can be formed over photoconductors 144 but prior to, and beneath, photoconductive layer 148. In this manner, photoconductive layer 148 is formed subsequent to formation of color resist layer 152, and overlying each color filter comprising color resist layer 152.

[0048] A separate nitride liner (not shown) can also be formed along the sidewall surfaces of each photoconductor 144 to guard against diffusion of impurities into the wafer or substrate 110 from the color filter materials comprising the color resist layer 152.

[0049] Turning to Figure 6, Figures 6A and 6B illustrate the present invention, at a stage subsequent to that shown in Figures 5A and 5B, respectively, after deposition of at least one photoconductive layer 156. Photoconductive layer 156 may be formed using one or more of the

photoconductive materials used in forming photoconductors 144, including for example nitride or silicon dioxide. Photoconductive layer 156 can be formed over color resist layer 152 and provides several advantages. For example, photoconductive layer 156 protects color resist layer 152 against damage during subsequent stages of CMOS imager formation, including but not limited to protection during backgrind, mount, saw, and die attach processing steps.

[0050] As illustrated schematically in Figures 7A and 7B, the sacrificial material 124 is then “decomposed” with a selection of proper materials to produce volatile products 170. During the decomposition process, any materials and conditions can be used that effectuate decomposition of the sacrificial material 124. The decomposition may be performed at temperatures anywhere in the range of about 125° C to about 200° C.

[0051] Addition of the proper decomposition materials, at a given temperature, causes sacrificial material 124 to produce volatile products 170. At this stage, the volatile products 170 of the decomposition then diffuse laterally and evaporate away from the silicon substrate and CMOS imager device. In another embodiment, an opening or “escape route” is formed for the removal of the volatile products 170.

[0052] Since color resist layer 152 can begin to decompose at high temperatures, for example, at approximately 250° C, it is preferred to decompose the sacrificial material 124 before the color resist layer 152 is formed.

[0053] Figures 8A and 8B illustrate in schematic form, after completion of the decomposition process, the completed CMOS imager with photoconductors 144 for light transmission to photo diodes 112. As depicted in Figures 8A and 8B, the space previously occupied by the

volatile products 170 is now occupied by at least one low refractive index material 180, for example, air ($n=1$). Other low refractive index materials 180 may also be used, as long as the refractive index (n value) of each photoconductor 144 is greater than the n value for each low refractive index material 180. The present invention therefore contemplates the use of other low refractive index materials besides air that fills the spaces between adjacent photoconductors 144. For example, at least one gaseous and/or non-gaseous fluidic materials may be used between adjacent photoconductors 144, as long as the refractive index (n value) of each photoconductor 144 is greater than the combined n value for the one or more gaseous and/or non-gaseous fluidic materials.

[0054] As depicted in Figures 9A and 9B, after removal of the volatile products 170 by evaporation and diffusion, each photoconductor 144 is separated by at least one low refractive index material 180. Since the refractive index (n) of each photoconductor 144 is greater than the refractive index (n) for each low refractive index material 180, light 190 entering each photoconductor 144 below certain angles will propagate within each photoconductor 144 to a photo diode 112 by total internal reflection. As depicted schematically in Figures 9A and 9B, this total internal reflection results in the “conduction” of light within each photoconductor 144 to a photo diode 112. Although one configuration of the invention is depicted in schematic form in Figures 9A and 9B, photoconductors 144 may be formed in any other configuration that results in propagation or “conduction” of light to photo diodes 112.

[0055] Figure 10 illustrates an exemplary processing system 900 which may utilize a memory device 100. Any one of the electronic components shown in Figure 10, including CPU 901 and memory device 100, may be fabricated as an integrated circuit for use in processing images formed in

accordance with the CMOS imaging devices and methods of the present invention. The processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0056] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device 100. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0057] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus

bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy device interface 920. The primary bus bridge 903 may also be coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0058] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0059] The processing system 900 illustrated in Figure 10 is only an exemplary processing system with which the invention may be used. While Figure 10 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a

variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory devices 100. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The photoconductor arrays and devices of the present invention, when coupled to a pixel processor, for example, may be implemented in digital cameras and video processors and recorders. Modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0060] While the invention is preferably directed to methods for forming photoconductors and photoconductor arrays and devices, and the resulting structures, one skilled in the art will recognize that the invention can be used to form any type of photoconductor array for integration with one or more processing components in a semiconductor device.

[0061] The present invention offers advantages over previous CMOS imaging technology, including, but not limited to, elimination of the need to use a ceramic package or lid attach in forming the CMOS imager. The instant methods for producing a CMOS imager also involve minimal power loss. Since no lens is required, the present invention eliminates concerns about lens radius limitations and about damaging lenses during die attach, backgrind, and mounting processes. The present invention also provides little or no cross talk between photo diodes.

[0062] It should again be noted that although the invention has been described with specific reference to CMOS imaging devices comprising a

structure for transmitting light to a photo diode, the invention has broader applicability and may be used in any CMOS imaging apparatus. Similarly, the process described above is but one method of many that may be used. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. Although certain advantages and preferred embodiments have been described above, those skilled in the art will recognize that substitutions, additions, deletions, modifications and/or other changes may be made without departing from the spirit or scope of the invention. Accordingly, the invention is not limited by the foregoing description but is only limited by the scope of the appended claims.